# Switched Doherty Power Amplifiers for CDMA and WCDMA

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*ABSTRACT* — **Power amplifiers for CDMA and WCDMA applications must provide competitive power efficiency at low power levels as well as at full power. This paper presents a novel approach that utilizes a modified Doherty architecture as a solution to this problem. PA ICs in both cellular and PCS bands are presented. Typical performance is -50dBc ACPR at PAE levels of 40% in high power mode (+28 dBm) and 21% in low power mode (+16.5 dBm). Design methodology, new cell geometry and manifold are also discussed.**

***Index Terms*** **— Doherty, HBT, Heterojunction bipolar transistors, Linear integrated circuits, MMIC power amplifiers, Power amplifiers.**

## I. Introduction

Power amplifiers for CDMA and WCDMA must operate over a wide range of output power. For example, much of the operating time of a CDMA PA is spent near +0 dBm. The low power DC to RF power conversion efficiency is an important factor in talk-time per battery charge.

Efficient PA operation can be achieved when the RF peak collector (or drain) voltage approximates the available DC supply voltage. A PA loaded for high power performance will suffer a loss in efficiency as the output power is reduced. Two choices are available to raise low power efficiency: 1.) adjust the DC voltage (to match the RF voltage), or 2.) adjust the load impedance and thereby the RF voltage. Load impedance modification avoids the additional cost, size and performance challenges that accompany a DC-DC converter. This is the choice we have made in this work.

Load impedance can be set *explicitly* through the "matching" network, and can be set *implicitly* by changing the relative degree of load sharing. Transistor cells in the final stage of a well designed power amplifier share the load uniformly. If some of the cells are not operational in a low power mode, the remaining active cells will view a lower impedance load. Clearly, switching off some of the final stage cells saves quiescent current in a low power mode; but, the resulting decrease in load impedance (per cell) causes a decrease in power efficiency. This can be seen in Fig. 1. Q1 represents a 1/M fraction of the total final stage periphery. This remains active in low power mode. Q2 is the remaining (M-1)/M fraction of the total periphery.

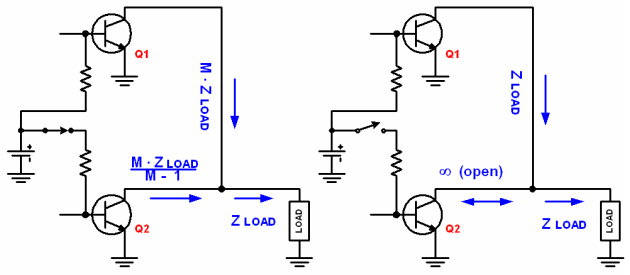



Fig.1 Load sharing in a periphery switched stage

For efficient low power operation, the increased loading of Q1, when Q2 is not contributing substantial output current, is a problem. Fig.2 illustrates the essential addition of an impedance inverter (as a quarter wave line) in the load path of Q1. This output network load split is one of the defining characteristics of a Doherty[1] power amplifier. In a conventional Doherty amplifier, there is no explicit switching of the bias. This is one of the differences in our switched Doherty approach.

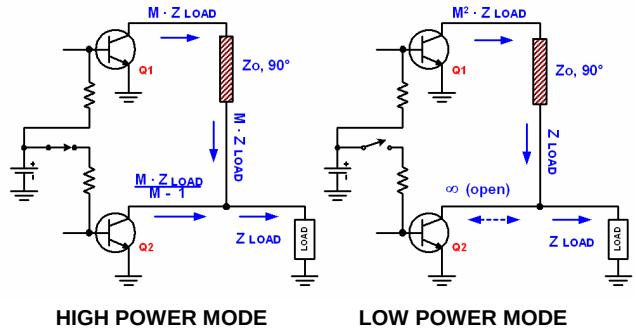



Fig.2 Load sharing in a switched Doherty stage

If the characteristic impedance of this line is matched to the optimum high power mode load for Q1, $M \cdot Z_{LOAD}$, then no additional impedance transformation results in that mode (only a 90° phase shift). However in the low power mode, when the loading of the Z inverter shifts downward to $Z_{LOAD}$, the loading of Q1 shifts upward to $M^2 Z_{LOAD}$. This upward shift in low power loading is responsible for the improved efficiency provided by Doherty amplifiers at backed-off power levels.

In recent years the Doherty amplifier has enjoyed renewed interest at microwave frequencies. Initially, solid state Doherty amplifiers were realized with FET[3] devices and later with HBTs[2,4].

Q1 and Q2 are of equal size when M=2. This is the classic form that W. H. Doherty investigated in 1936. The parameter M is also sometimes called γ. Cases in which M>2 are sometimes called *Extended Doherty Amplifiers* [2]. As M is increased, the transition point from low power to high power is reduced. This transition point is approximately 20·log(M) below the full power level. For CDMA handset PAs, M is usually in the range of 3-4.

The phase shift that the impedance inverter introduces between Q1 and the current summing node must be also applied to the drive signal into Q2. In this way, the high power mode output currents will add in-phase. In a conventional Doherty amplifier this input phase difference is accomplished with a quadrature hybrid or an in-phase hybrid (such as a Wilkinson) and a 90° delay line.

## II. Approach

Our approach uses a modified Doherty architecture:

1. Both Q1 and Q2 are operated in class AB mode. This is necessary for linearity performance required for CDMA operation. A conventional Doherty with the class C peaking amplifier will not support this.
2. The impedance inverter is defined based on the low power requirement. Since the high power load for Q1 is the same as the inverter impedance, the size of Q1 is implied as a fraction of the total stage transistor (Q1+Q2). Q1 and Q2 are usually not equal.
3. Part of Q1 periphery is also switched off during low power mode. This is for optimum sizing of the active transistor. Recall, Q1 was set consistent with the impedance requirements the target low power output level. This is usually larger than required. Essentially, this modification provides 2 degrees of design freedom allowing both the low power mode periphery and load Z to be set independently. This is significant.
4. The impedance inverter and delay line are realized as lumped equivalent circuits. The relationship to λ/4 line parameters is shown in Fig.3 and Fig.4. ωo is the 90° frequency. Delay lines use the constant-k form. Second harmonic shorts are provided by the m-derived form, as seen in Fig.4.
5. A 4-port hybrid is not used in the interstage drive splitter, primarily due to area considerations.
6. The interstage match design is obtained by first doing a match for a conventional PA with the same number of driver and final cells. The first step in the transformation (starting at the base side of the final) is partitioned by impedance scaling according to the Q1 and Q2 sizes. The delay-line impedance is designed to match the impedance provided by the transformed high power side (Q2) input.

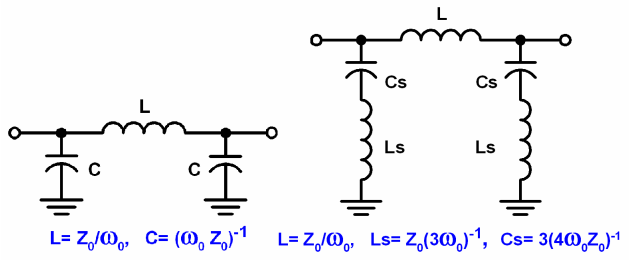



Fig.3 Lumped equivalent *constant-k* impedance inverter




Fig.4 Lumped equivalent *m-derived* impedance inverter with 2nd harmonic short circuit.

This approach offers several distinct advantages over other load line shift methods. Firstly, the entire available periphery is being utilized in the high power mode, while in the low power mode, some of periphery is simply turned off. This is in contrast to other methods that often have unused periphery in both modes, consequently, requiring low loss RF switches. The second advantage is the improvement of load insensitivity. This is a result of the quadrature operation that naturally occurs from the impedance inverter and delay line. Yet the third advantage is the preservation of transmission phase through power mode changes.

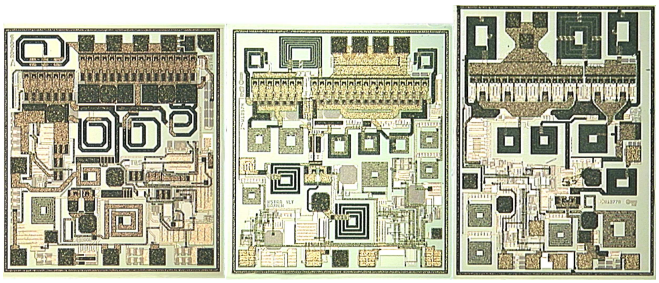
## III. FEATURES

The first generation switched Doherty PA was designed for the PCS band and completed in 2004 (our patent filed in 2002). These chips have successful in a number of key sockets. A second generation to this PA was developed in 2006. Both of these chips are shown in Fig.5.

Some of the innovations contained in these chips are: absorption of harmonic tuning into the inverter on both sides; use of low Zo Au/BCB/Au transmission lines to reduce inductance in the base manifold; overlay coupled split inductors improve the Q·L/A figure of merit;, and a new fishbone base HBT geometry to substantially reduce $C_{BC}$ and thereby improve the linear power efficiency.

The interstage matching networks in the second generation designs consider the second harmonic impedance interface to the base of the output stage in addition to the fundamental frequency. This is an important factor in linearity performance. Fig.5 illustrates two of the viable interstage topologies in second

generation chips. They are both bandpass in contrast with the highpass approach in first generation chips.



(1120 x 1200 um$^2$) (1170 x 1230 um$^2$) (1120 x 1470 um$^2$)

**1ST GEN PCS** **2ND GEN PCS** **2ND GEN CELL**

Fig.5 First and second generation switched Doherty PAs.

Significantly, the delay-line, Z-inverter, and harmonic tuning inductors have been integrated into the cellular PA chips. Clearly, these elements can consume considerable module area if placed externally. A more important result is: these fully integrated solutions can be used in modules that were designed for conventional PAs, since the external matching circuit is the same as for a conventional PA.

The *fishbone base* HBT geometry shown in Fig.6 was used in both generations of these PAs. Low collector-base capacitance is the key device parameter in achieving highly linear and power efficient amplifier performance. As a relative $C_{CB}$ figure of merit, the ratio of emitter area to base (mesa) area is important, and should be as large as possible (always <1). The *fishbone base* cell used in these PAs has $E_A/B_A$ = 0.42. This represents less than 500 fF/mm at 3.4V (20% improvement over our standard cell).

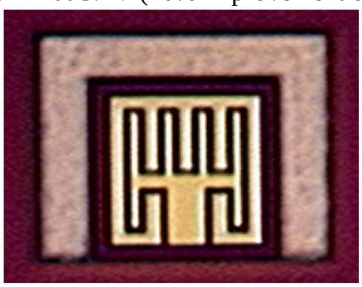


Fig.6 *Fishbone-Base* geometry with low $C_{BC}$

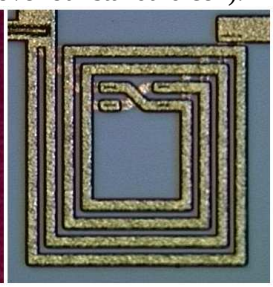


Fig. 7 Multilayer (overlay) split inductor

Another figure of merit related to $R_B$' considers the amount of emitter periphery in the base area. The *fishbone base* cell has $E_P/(B_A)^{½}$ = 9.2 Again, a significant gain of 8% over our standard geometry is observed.

The second generation designs each have substantial inductive content in the interstage networks. Fig.7 shows an innovative 2 layer coupled inductor with split lines in each plane. This inductor was used in the second generation PCS PA. It provides both layout area efficiency and Q improvement over conventional broadside coupled inductors.

RF drive and loading should be uniform across all cells in a common block (Q1 or Q2). The Triquint HBT process provides several layers of gold and BCB ($\varepsilon_r$~2.6) for interconnect. We use the BCB interlayer dielectric to provide a low Zo transmission line for the base feed manifold to minimize the interconnect path inductance. More significantly, *differences* in interconnect path inductance across the array of HBT cells are reduced. An example of this is shown in Fig.8. A finite ground width microstrip is formed between metal-2 and metal-1 (separated by BCB). Substrate vias are placed below the metal-1 ground-plane. This approach allows nearly an order of magnitude reduction in manifold inductance. A small penalty in shunt capacitance is the tradeoff.

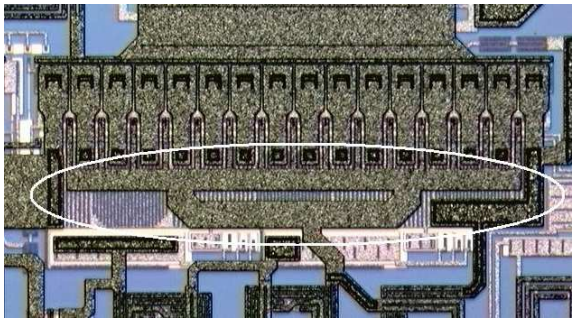


Fig.8 Low inductance base manifold provided by Zo transmission line (~ microstrip on thin BCB).

## IV. Results and Summary

The switched Doherty amplifiers have been tested in both PCS and cellular bands with IS-98 CDMA, 3GPP rel.99, and HSDPA WCDMA modulations.

IS-98 CDMA performance in PCS band is 40 % PAE, -51 dBc ACPR, and -59 dBc AltCPR all at 28 dBm, as shown in Fig.9. In the low power mode, the PAE is 20 % at 16 dBm with ACPR of -57 dBc and AltCPR of -60 dBc. When driven up to 16.5 dBm, the amplifier operates at 21.5% PAE, -52.5 dBc ACPR and -58 dBc AltCPR.

In the cellular band, the amplifier delivers 28 dBm with 40 % PAE, -50 dBc ACPR and -58 dBc AltCPR. In the low power mode, 19.5 % PAE is obtained at 16 dBm with -52 dBc ACPR and -68 dBc AltCPR. At 16.5 dBm, ACPR and AltCPR can still uphold -50 dBc and -67 dBc with 20.5 % PAE.

Gains are quite flat at +27 dB / +19 dB in PCS and +26 dB / +23.5 dB in cellular.

The PA chips were also characterized with WCDMA modulations, both 3GPP rel.99 and HSDPA. Fig.10 shows the 3GPP rel.99 PCS performance to be 43 % PAE at 29 dBm with ACPR of -41 dBc and AltCPR of -56 dBc. In the low power mode the PAE is 24 % at 18 dBm with -41 dBc ACPR and -56 dBc AltCPR. For HSDPA, the amplifier can demonstrate 39 % PAE, -41.5 dBc ACPR and -58 dBc AltCPR at 28 dBm in high power, and 22 % PAE, -41 dBc ACPR and -58 AltCPR at 16.5 dBm.

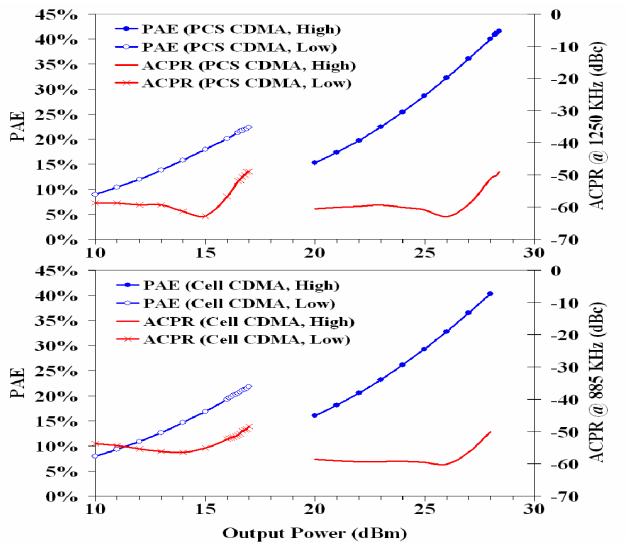



Fig. 9 Measured PAE and ACPR@1250KHz offset with IS-98 CDMA, Freq=1880 MHz and 836.5 MHz.

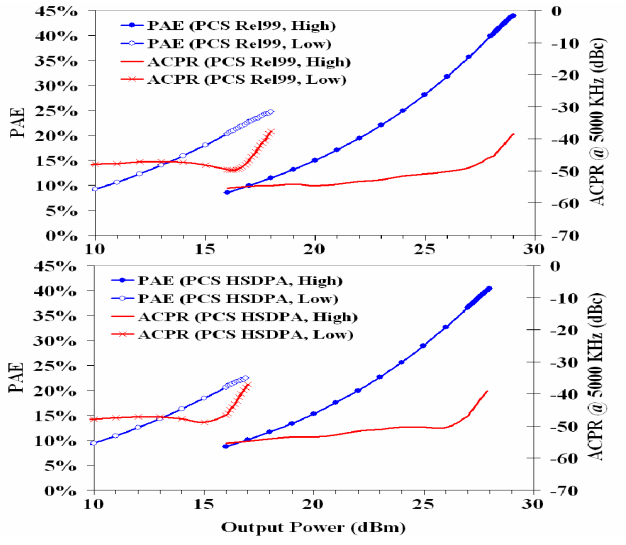



Fig. 10 Measured PAE and ACPR@5MHz offset with WCDMA 3GPP rel.99 and HSDPA, Freq=1880 MHz.

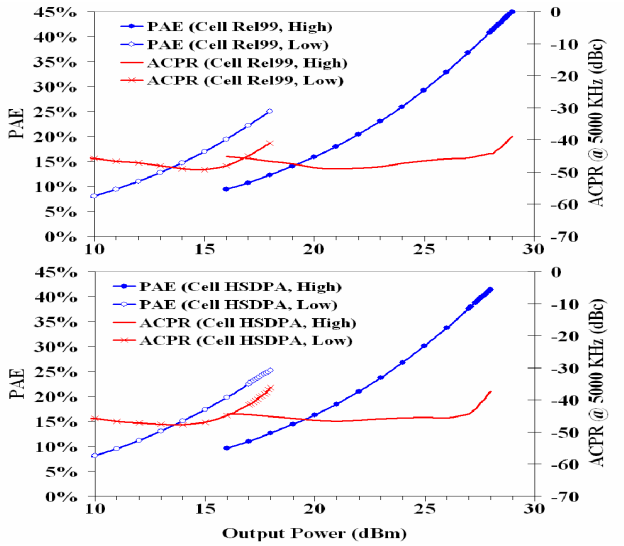



Fig. 11 Measured PAE and ACPR@5MHz offset with WCDMA 3GPP rel.99 and HSDPA, Freq =836.5 MHz.

The WCDMA performance in the cellular band is shown in Fig.11. With 3GPP rel.99, the PA can achieve 44% PAE at 29 dBm with -40.5 dBc ACPR and -55 dBc AltCPR, and 25 % PAE, -41 dBc ACPR and -63 dBc AltCPR at 18 dBm. The HSDPA performance is 40 % PAE, -40.5 dBc ACPR and -57.5 dBc AltCPR at 27.5 dBm, and 22.5 % PAE, -42.5 dBc ACPR and -62 AltCPR at 17 dBm.

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